ACSER
AUSTRALIAN CENTRE FOR SPACE ENGINEERING RESEARCH

THE UNIVERSITY OF NEW SOUTH WALES
SYDNEY · AUSTRALIA

PhD Scholarship at Australian Centre for Space Engineering Research

Required Background:	Bachelor/Master's Degree in Electronics/Computer Engineering
Keywords:	Re-configurable Processing, FPGA, Signal Processing
Preferred Experience:	FPGA, Signal Processing
Application Deadline:	31/03/2012
Supervisors:	Dr Ediz Cetin, Dr Oliver Diessel
Contact:	Dr Ediz Cetin (e.cetin@unsw.edu.au)

SEU Detection and Mitigation for Satellite Based FPGA On-board Processing

Future earth observation missions are expected to have very high data rate and processing requirements. The next generation of on-board processing is also required to be flexible and re-programmable in-orbit and during active service. This brings about challenging requirements for future on-board processing systems that cannot be met with space-qualified processors available today. Commercial-Off-The-Shelf (COTS) Field Programmable Gate Arrays (FPGAs) provide a viable solution to meet these stringent requirements however they suffer from radiation-induced Single Event Upsets (SEUs). Given their reliance on configuration memory, FPGAs are more prone to these upsets when compared to Application Specific Integrated Circuits (ASICs). SEUs manifest themselves in the form of Single-Bit Upsets (SBUs), where only one bit is affected by the SEU. However, with diminishing transistor sizes the likelihood of a proton or heavy ion causing Multi-Bit Upsets (MBUs) rather than just SBUs due to SEUs increases. Hence, detection and mitigation of effects of SEUs for satellite-based FPGA systems is of paramount importance.

The research work is concerned with proposing novel solutions to mitigate effects of the SEUs on FPGAs. Research will start with analysing fault injection methods to model and characterise SEU effects on COTS FPGAs. This will be followed by developing innovative low-complexity methods for detecting and localizing SBU/MBUs due to SEUs in the system. The research will culminate in the development of novel run-time low-complexity SEU mitigation techniques, thereby paving the way for widespread use of FPGAs for space applications.

ACSER will be providing scholarships for some students. All prospective students should, however, apply for:

- Australian Postgraduate Award (APA; for Australian citizens) OR an
- International Postgraduate Research Scholarship (IPRS; International students).

Suitability for the ACSER scholarships will be assessed in the same way as applicants for APA and IPRS. For more information about these scholarships please go to http://research.unsw.edu.au/postgraduate-research-scholarships.

Further Information on the project may be obtained from Dr Ediz Cetin (e.cetin@unsw.edu.au)